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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/890,120	07/27/2001	Jean-Luc Pelloie	025219-336	5893

7590 09/23/2003

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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/890,120	Applicant(s) Pelloie Et.al.
	Examiner Edgardo Ortiz	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 11, 2003* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-11* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to an amendment filed July 11, 2003 in which Applicant amended claim 1.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5 and 6 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Douseki (U.S. Patent No. 5,821,769) in view of Kim (U.S. Patent No. 6,121,079). With regard to Claim 1, Douseki teaches a MOS transistor (M1) having a gate (23) and a channel (24) of a first conductivity type (p), a first doped zone (25) of a first conductivity type coupled to the channel of said first MOS transistor and a current limiter (M2) coupled between the gate of said MOS transistor and said first doped zone, said current limiter comprising a second doped zone (26) of a second conductivity type (n+) in ohmic contact (30) with said first doped zone. See figure 9A.

However, Douseki fails to teach a second doped zone of a second conductivity physically disposed against the first doped zone. Kim discloses a semiconductor memory device including gates (17D) and junction regions (19-1, 19-2, 19-3, 19-4, 19-5, 19-6, 19-7), wherein junction region (19-4) comprises two regions of first and second conductivity types, physically disposed

against each other (column 6, lines 53-67; column 7, lines 1-2 and figure 6B). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Douseki to include a second doped zone of a second conductivity physically disposed against the first doped zone, as clearly suggested by Kim, in order to reduce implantation process steps when creating the first and second doped zones (column 7, lines 7-10).

With regard to Claim 2, Douseki teaches a current limiter (M2) comprising a second transistor, the second doped zone (26) embodying the source of said second transistor.

With regard to Claim 4, Douseki teaches a second transistor (M2) that has a gate (28) coupled to the second doped zone (26).

With regard to Claim 5, Douseki teaches a terminal (B) that is coupled to the gate of the second transistor (M2) and to the second doped zone (26).

With regard to Claim 6, Douseki teaches a drain (27) of the second transistor (M2) that is coupled to the gate (23) of the first MOS transistor (M1).

Claim 3 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Douseki (U.S. Patent

No. 5,821,769) in view of Kim (U.S. Patent No. 6,121,079) and further in view of Hu et.al. (International Application WO 96/07205). Douseki and Kim, as stated supra, essentially discloses the claimed invention but fails to show, a gate polarization terminal coupled to the gate of the second transistor. Hu discloses a MOS transistor (32) connected to a second transistor (30) that provides an external bias and which has a gate polarization terminal (gate voltage) coupled to its gate. See Figure 15. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Douseki and Kim to include a gate polarization terminal coupled to the gate of the second transistor, as clearly suggested by Hu, in order to improve the current drive of a MOS transistor (column 8, lines 20-21).

Claims 7-11 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Douseki (U.S. Patent No. 5,821,769) in view of Kim (U.S. Patent No. 6,121,079) and further in view of Voldman et.al. (U.S. Patent No. 6,015,993). Douseki teaches a current limiter (M2) including a second doped zone (26) embodying a first terminal and a third doped zone (27) embodying a second terminal of the current limiter. See figure 9A.

However, Douseki fails to show that the current limiter comprises a diode wherein the second and third doped zones are of opposite conductivity type. Voldman discloses a FET diode structure including doped zones (142, 144) which embody the terminals of the diode and are of

opposite conductivity type. See figure 2. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Douseki and Kim to include current limiter comprising a FET diode structure and doped zones which embody the terminals of the diode and of opposite conductivity type, as clearly suggested by Voldman, in order to withstand high voltage (column 3, lines 50-60).

With regard to Claim 8, Douseki teaches a fourth doped zone (29) disposed between the second (26) and third (27) doped zones, said fourth doped zone having the same conductivity type as the conductivity type of either the second or third zones.

With regard to Claim 9, Douseki teaches a third doped zone (27) coupled to the gate (25) of the first MOS transistor (M1).

With regard to Claim 10, Douseki teaches a gate (28) extending over the fourth doped zone (29).

With regard to Claim 11, Douseki teaches a gate (28) coupled to one of the terminals (26).

Response to Arguments

2. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

9/16/03

GEORGE ECKERT
PRIMARY EXAMINER